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10/727,138	12/03/2003	Kaushik Saha	852463.406	5322

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,138	SAHA ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 11/09/2007.

2. Claims 1-20 are pending in this application. Claims 1, 3, 5, and 16 are independent claims. This Office Action is made final.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, limitations cited in claims 8-9, particularly the radix-size, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-20 cite a method, system, product, and medium for performing a/an FFT/IFFT in accordance with a predetermined mathematical algorithm. However, claims 1-20 merely disclose steps/components for performing FFT/IFFT without disclosing a practical/physical application and further the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein. In addition, claims {3-4 and 12-15} can be seen as software module; claims 5-6 are software per se. and claims 16-20 are non-functional medium. Therefore, claims 1-20 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abel et al. (U.S. 5,991,787) in view of Jaber (U.S. 6,792,441).

Re claim 1, Abel et al. disclose in Figures 1-14 a linear scalable method for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a system (e.g. abstract, Figures 7 and 11 wherein Figure 7 discloses an IFFT and Figure 11 discloses a FFT) using a decimation in time approach (e.g. last line of abstract and col. 13 line 65 to col. 14 line 12), comprising the steps of: computing an N-point FFT/IFFT of a signal (e.g. either seen in Figures 7-8 or Figure 11 for IFFT/FFT respectively) using a first plurality of butterfly computational stages (e.g. Figure 4 and Figure 8 wherein the first plurality of butterfly is performed in components 800 and 805), each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix (e.g. Figure 8 wherein components 800 and 805 each utilizes radix-2 as the first radix size) wherein each of the butterfly operations in each stage (e.g. components 800, 805, and 810 in Figure 8) in the first plurality of stages has a single, un-nested computation loop of the first radix (e.g. Figure 4 and Figure 8 wherein there is no loopback/feedback for computing the IFFT/FFT); and storing the transformed signal (e.g. Figures 15-16 and col. 13 lines 10-45).

Abel et al. fail to disclose in Figures 1-14 the multiprocessing system for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage. However, Jaber discloses in Figures 8-9 the multiprocessing system (e.g. Figure 8 or Figure 9 as multiprocessing system for FFT/IFFT) for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage (e.g. abstract and col. 3 lines 30-68 wherein the input data is breakdown in block corresponding to each processor for computing Fourier Transform).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiprocessing system for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and simultaneously (e.g. abstract and summary of the invention in cols. 3-4).

Re claim 2, Abel et al. fail to disclose in Figures 1-14 step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor. However, Jaber discloses in Figures 8-9 step of distributing butterfly operations in each

stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor (e.g. col. 7 lines 2-30).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and independent from each other (e.g. abstract and col. 6 line 60 to col. 7 line 30).

Re claim 3, it is a system claim of claim 1. Thus, claim 3 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 4, it is a system claim of claim 2. Thus, claim 4 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 5, it is a program product claim of claim 8. Thus, claim 5 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 6, it has similar limitations cited in claim 2. Thus, claim 6 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 7, Abel et al. further disclose in Figures 1-14 the first radix is a radix-2 radix (e.g. component 800 in Figure 8 wherein the component 800 utilizes radix-2 to compute the butterfly computation of IFFT).

Re claim 8, Abel et al. further disclose in Figures 1-14 the first plurality of stages comprises $\log_2 N$ minus two stages (e.g. as ($\log_2 N$) - 2 stages are seen in component 800 in Figure 8), further comprising computing a first and second stage of $\log_2 N$ stages of the N-point FFT/IFFT as a single radix-4 butterfly operation (e.g. component 900 in Figure 9).

Re claim 9, Abel et al. further disclose in Figures 1-14 the first plurality of stages comprises $\log_2 N$-2 stages (e.g. Figure 4 and Figure 8).

Re claim 10, Abel et al. further disclose in Figures 1-14 an output of a last stage in the first plurality of stages provides the computed N-point FFT/IFFT (e.g. output of Figure 4 or Figure 8).

Re claim 11, Abel et al. fail to disclose in Figures 1-14 the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location. However, Jaber discloses in Figures 8-9 the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location (e.g. col. 15 lines 4-35).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and independent from each other (e.g. abstract and col. 6 line 60 to col. 7 line 30).

Re claim 12, it is a system claim of claim 7. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 13, it is a system claim of claim 8. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 14, it is a system claim of claim 9. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 15, it is a system claim of claim 11. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 16, it is a computer-readable memory claim of claim 1. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 17, it is a computer-readable memory claim of claim 2. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 18, it is a computer-readable memory claim of claim 11. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 19, it is a computer-readable memory claim of claim 9. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 20, it is a computer-readable memory claim of claim 10. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Response to Arguments

8. Applicant's arguments filed 11/09/2007 have been fully considered but they are not persuasive.

a. The applicant argues in page 6 for claims rejected under 35 U.S.C. 101 that the claims disclose a step of storing the transformed signal. This step would constitute as a tangible result thus it satisfies the requirement under 101. Further, other independent claims have similar limitations addressed above, thus other independent claims also produce a useful, tangible, and concrete result.

The examiner respectfully submits that the step of storing transformed signal can not constitute or consider as useful, concrete, and tangible as alleged by the applicant. A tangible result is a real world or practical result which provide a practical application. Generally, these claims lack of a practical application and preempt substantial practical applications. Further, claims {3-4 and 12-15} can be seen as software module due the means; claims 5-6 can be seen as software per se. due to program on medium without executing. and claims 16-20 further can be seen as non-functional medium since the any "contents" of medium cannot cause the system to perform FFT/IFFT as claimed.

b. The applicant argues in page 7 second paragraph for claims rejected under 35 U.S.C. 103(a) that the primary reference by Abel fails to disclose "a linear scalable method" as cited in the preamble of the claims.

The examiner respectfully submits that the primary reference by Abel does disclose the linear scalable method of performing FFT/IFFT as clearly seen in Figure 7 wherein input data coefficients can be any size.

In addition or alternative to the response, the recitation "a linear scalable method" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

c. The applicant argues in page 7 third paragraph for claims 1 and 16 rejected under 35 U.S.C. 103(a) that neither Abel nor Jaber teach, suggest, or motivate a linear scalable method comprising a first plurality of stages employing a plurality of butterfly operations having a first radix, wherein each of the butterfly operations in each stage in the first plurality of stages has a single, un-nested computation loop of the first radix as recited in the claim. Similarly argument is also applied to other independent claims in pages 7-8.

The examiner respectfully submits that the primary reference by Abel clearly discloses the above argued limitations as clearly addressed as below:

Abel et al. disclose in Figures 1-14 a linear scalable method for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a system (e.g. abstract, Figures 7 and 11 wherein Figure 7 discloses an IFFT and Figure 11 discloses a FFT) using a decimation in time approach (e.g. last line of abstract and col. 13 line 65 to col. 14 line 12), comprising the steps of: computing an N-point FFT/IFFT of a signal (e.g. either seen in Figures 7-8 or Figure 11 for

IFFT/FFT respectively) using a first plurality of butterfly computational stages (e.g. Figure 4 and Figure 8 wherein the first plurality of butterfly is performed in components 800 and 805), each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix (e.g. Figure 8 wherein components 800 and 805 each utilizes radix-2 as the first radix size) wherein each of the butterfly operations in each stage (e.g. components 800, 805, and 810 in Figure 8) in the first plurality of stages has a single, un-nested computation loop of the first radix (e.g. Figure 4 and Figure 8 wherein there is no loopback/feedback for computing the IFFT/FFT); and storing the transformed signal (e.g. Figures 15-16 and col. 13 lines 10-45).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

January 8, 2008